IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of)
)
HAYASHI et al.)
)
Application Number: To Be Assigned)
)
Filed: Concurrently Herewith)
)
For: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Applicant has amended the claims in order to remove multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment. Prior to an examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Please substitute the claims currently on file with the following amended claims:

5. (Amended) A level conversion circuit according to Claim 1, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

6. (Amended) A level conversion circuit according to Claim 1, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the

ratio between the gate width and the gate length of said first n-channel type MOS transistor.

Please add the following new claims:

20. A level conversion circuit according to Claim 4, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

21. A level conversion circuit according to Claim 5, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

22. A level conversion circuit according to Claim 20, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

REMARKS

Applicant has amended claim 5 and added claim 20, and amended claim 6 and added claims 21 and 22. Applicant has amended the claims in order to remove multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment.

In view of the above amendments and Applicant's comments stated herein, Applicant respectfully requests an early and favorable action on the merits.

Respectfully submitted,

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Marked Up Version of the Claims

5. A level conversion circuit according to Claim~~s~~ 1 ~~or 4,~~ wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

6. A level conversion circuit according to Claim~~s~~ 1 ~~or 5,~~ wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.